WHAT IS CLAIMED IS:

1. A method of forming a thin film transistor liquid crystal display (TFT-LCD) on a substrate, comprising the steps of:

forming a first stack structure and a second stack structure on the substrate, the first stack structure comprises layers successively disposed which are a first conduction layer, a first insulation layer, a first semiconductor layer, a first ohmic contact layer, and a first photoresist layer, the second stack structure comprises layers successively disposed which are a second conduction layer, a second insulation layer, a second semiconductor layer, a second ohmic contact layer, and a second photoresist layer, wherein the first photoresist layer has a first thickness, and the second photoresist layer has a second thickness which is smallerthan the first thickness;

ashing the first and the second photoresist layers and removing at least the second ohmic contact layer, the second semiconductor layer to form a third stack structure and a fourth stack structure, wherein the third stack structure comprises the first conduction layer, the first insulation layer, the first semiconductor layer, the first ohmic contact layer, and a third photoresist layer, and the fourth stack structure comprises at least the second conduction layer;

forming a third insulation layer on the substrate;

lifting off the third photoresist layer to remove the third insulation layer on the third photoresist layer;

forming a third conduction layer on the substrate;

patterning the third conduction layer to expose a part of the first semiconductor layer and the third insulation layer on the fourth stack structure and to form drain and source electrodes;

forming a passivation layer on the substrate;

patterning the passivation layer and the third insulation layer to expose a part of the third conduction layer and a part of the second conduction layer; and

forming a transparent conduction layer on the passivation layer and the third conduction layer, wherein a first part of the transparent conduction layer is used to be a pixel electrode connecting to the third conduction layer, and a second part of the transparent conduction layer is connected to the second conduction layer.

2. The method according to claim 1, wherein the step of lifting off the third photoresist layer is conducted by wet etching.

3. The method according to claim 1, wherein the third insulation layer is made of silicon nitride.

4. The method according to claim 1, wherein the first conduction layer and the second conduction layer are gate electrodes.

5. A method of forming a thin film transistor liquid crystal display on a substrate, comprising the steps of:

forming a stack structure on the substrate, wherein layers of the stack structure successively disposed are a first conduction layer, a first insulation layer, a first semiconductor layer, a first ohmic contact layer, and a photoresist layer, and the stack structure is patterned by using the photoresist layer as a mask;

forming a second insulation layer at least on sidewall of the stack structure;

forming a second conduction layer on the substrate;

patterning the second conduction layer to expose a part of the semiconductor layer and to form a drain electrode and a source electrode;

forming a passivation layer on the exposed semiconductor layer and a

part of the second conduction layer; and

forming a transparent conduction layer on the passivation layer to electrically connect to the second conduction layer.

6. The method according to claim 5, wherein the second insulation layer is formed of silicon nitride.

7. The method according to claim 5, wherein the first conduction layer and the second conduction layer are gate electrodes.

8. The method according to claim 5, wherein the step of forming a second insulation layer further comprises the following steps:

forming a second insulation layer on the substrate; and

lifting off the photoresist layer to remove the second insulation layer on the photoresist layer.

9. The method according to claim 8, wherein the step of lifting off the photoresist layer is conducted by wet etching.

10. A thin film transistor substrate, comprising at least:

a first stack structure and a second stack structure on the substrate,

wherein the first stack structure comprises layers successively disposed which are a first conduction layer, a first insulation layer, and a semiconductor layer, and the second stack structure at least includes a second conduction layer;

an ohmic contact layer on a first region and a second region of the semiconductor layer, where the first region and the second region are disconnected;

a second insulation layer, positioned at least on the side surfaces of the first stack structure and the second stack structure and a part of the upper surface of the second stack structure;

a source electrode and a drain electrode, wherein the source electrode is positioned on a part of the second insulation layer and the ohmic contact layer in the first region, and the drain electrode is positioned on a part of the second insulation layer and the ohmic contact layer in the second region;

a passivation layer, positioned on the semiconductor layer, the source and the drain electrodes, and the second insulation layer; and

a transparent conduction layer, disposed on the passivation layer, wherein a first portion of the transparent conduction layer is electrically

coupled to one of the source and the drain electrode and a second portion of the transparent conduction layer is electrically coupled to the second conduction layer of the second stack structure.

11. The substrate according to claim 10, wherein the second insulation layer is further deposited between the first stack structure and the second stack structure.

12. The substrate according to claim 10, wherein the first portion and the second portion of the transparent conduction layer is disconnected.

13. The substrate according to claim 10, wherein the first portion and the second portion of the transparent conduction layer is connected.

14. The substrate according to claim 10, wherein the first conduction layer and the second conduction layer are gate electrodes.

15. The substrate according to claim 10, wherein the transparent electrode layer is formed of indium-tin-oxide (ITO).

16. A thin film transistor substrate, comprising at least:

a plurality of stack structures on the substrate, wherein each stack structure comprises layers successively disposed which are a first conduction

layer, a first insulation layer, and a semiconductor layer;

an ohmic contact layer, positioned on a first region and a second region of the semiconductor layer, where the first region and the second region are disconnected;

a second insulation layer, positioned at least on side surfaces of the stack structures;

a source electrode and a drain electrode, wherein the source electrode is positioned at least on the ohmic contact layer in the first region, and the drain electrode is positioned at least on the ohmic contact layer in the second region;

a passivation layer, positioned on the semiconductor layer and the source and the drain electrodes; and

a transparent conduction layer, positioned on the passivation layer and electrically coupled to one of the source and the drain electrodes.

17. The substrate according to claim 16, wherein the second insulation layer is further deposited among the stack structures.

18. The substrate according to claim 16, wherein the second insulation

layer is formed of silicon nitride.

19. The substrate according to claim 16, wherein the first conduction layer is a gate electrode.

20. The substrate according to claim 16, wherein the transparent electrode layer is formed of indium-tin-oxide.

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